CLAIMS

1. A temperature independent CMOS reference voltage circuit, comprising:

a CMOS current mirror circuit containing first and second CMOS transistors of a first polarity; and

a temperature compensation circuit coupled to said CMOS current mirror circuit, and containing a first resistor, a second resistor, and third and fourth CMOS transistors of a second polarity.

2. The temperature independent CMOS reference voltage circuit according to claim 1, wherein said third and fourth CMOS transistors are configured to operate substantially in a subthreshold region.

3. The temperature independent CMOS reference voltage circuit according to claim 1, wherein one of said third and fourth CMOS transistors is diode connected.

4. The temperature independent CMOS reference voltage

circuit according to claim 1, wherein said fourth CMOS transistor is diode connected.

5. The temperature independent CMOS reference voltage circuit according to claim 1, wherein at least one of said first and second resistors is variable.

6. The temperature independent CMOS reference voltage circuit according to claim 1, wherein said first resistor is coupled between sources of said third and fourth CMOS transistors.

7. The temperature independent CMOS reference voltage circuit according to claim 1, wherein gates of said third and fourth CMOS transistors are interconnected.

8. The temperature independent CMOS reference voltage circuit according to claim 1, wherein:

a first side of said second resistor is coupled to drain of said fourth CMOS transistor; and

a second side of said second resistor is coupled to said CMOS current mirror circuit for generating a reference

voltage substantially unaffected by temperature changes.

9. The temperature independent CMOS reference voltage circuit according to claim 1, wherein said temperature compensation circuit is configured to generate a reference voltage containing a proportional to absolute temperature (PTAT) voltage component and a threshold voltage of said fourth CMOS transistor.

10. The temperature independent CMOS reference voltage circuit according to claim 9, wherein said PTAT voltage component and said threshold voltage have complementary temperature coefficients.

11. The temperature independent CMOS reference voltage circuit according to claim 9, wherein said PTAT voltage component has a positive temperature coefficient and said threshold voltage has a negative temperature coefficient causing the reference voltage to be substantially unaffected by temperature changes.

12. The temperature independent CMOS reference voltage circuit according to claim 11, wherein said positive temperature coefficient is proportional to kT/q.

13. The temperature independent CMOS reference voltage circuit according to claim 1, wherein said first and second CMOS transistors are PMOS transistors and said third and fourth CMOS transistors are NMOS transistors.

14. The temperature independent CMOS reference voltage circuit according to claim 1, wherein said first and second CMOS transistors are NMOS transistors and said third and fourth CMOS transistors are PMOS transistors.

15. The temperature independent CMOS reference voltage circuit according to claim 1, wherein said CMOS current mirror circuit is configured as one of a cascode circuit and a gain boosted circuit.

16. A CMOS temperature compensation circuit, comprising:

first and second CMOS transistors having interconnected gates and configured to operate substantially in a subthreshold region, said second CMOS transistor being diode connected;

a first resistor coupled between sources of said first

and second CMOS transistors; and

a second resistor having a first end coupled to drain of said second CMOS transistor and having a second end coupled to a current mirror circuit for generating a reference voltage that is substantially unaffected by temperature changes.

17. The CMOS temperature compensation circuit according to claim 16, wherein said first resistor and said second resistor are variable.

18. The CMOS temperature compensation circuit according to claim 16, wherein the reference voltage contains a proportional to absolute temperature (PTAT) voltage component and a threshold voltage of said second CMOS transistor.

19. The CMOS temperature compensation circuit according to claim 18, wherein said PTAT voltage component and said threshold voltage have complementary temperature coefficients.

20. The CMOS temperature compensation circuit according to

claim 19, wherein said PTAT voltage component has a positive temperature coefficient and said threshold voltage has a negative temperature coefficient causing the reference voltage to be substantially unaffected by temperature changes.

21. The CMOS temperature compensation circuit according to claim 20, wherein said positive temperature coefficient is proportional to kT/q.

22. The CMOS temperature compensation circuit according to claim 16, wherein said first and second CMOS transistors are NMOS transistors.

23. The CMOS temperature compensation circuit according to claim 16, wherein said first and second CMOS transistors are PMOS transistors.

24. An integrated temperature independent CMOS reference voltage circuit, comprising:

a substrate having a CMOS current mirror circuit containing first and second CMOS transistors of a first polarity; and

a temperature compensation circuit coupled to said CMOS current mirror circuit, and containing a first resistor, a second resistor, and third and fourth CMOS transistors of a second polarity.

25. An integrated CMOS temperature compensation circuit, comprising:

a substrate having first and second CMOS transistors with interconnected gates and configured to operate substantially in a subthreshold region, said second CMOS transistor being diode connected;

a first resistor coupled between sources of said first and second CMOS transistors; and

a second resistor having a first end coupled to drain of said second CMOS transistor and having a second end coupled to a current mirror circuit for generating a reference voltage that is substantially unaffected by temperature changes.